UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/428,134	10/26/1999	JASMIN AJANOVIC	042390.P6341	4288

7590 03/01/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 900251026

EXAMINER	
AUVE, GLENN ALLEN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/428,134	AJANOVIC ET AL.	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-20,22-30,32-35 and 37-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-20,22-30,32-35 and 37-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant should note that the examiner in charge of this application has changed. The current contact information is included at the end of this Office Action.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4-7,12,13,22-27,30-49, and 62-64 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 is rejected based on lack of positive antecedent basis of "said request packet" on lines 1-2.

Claims 7 and 13 are rejected because they depend on claim 4.

Claim 5 is rejected based on lack of positive antecedent basis of "said request packet" on line 2 and "said first transaction" on lines 2-3.

Claim 6 is rejected based on lack of positive antecedent basis of "said request packet" on lines 1-2 and "said completion packet" on line 2.

Claim 7 is rejected based on lack of positive antecedent basis of "said request packet" on line 3 and "said first transaction" on line 3.

Claim 12 is rejected based on lack of positive antecedent basis of "said transaction descriptors" on line 1.

Claim 13 is rejected based on lack of positive antecedent basis of "said request packet" on line 1 and "the respective request packet" on lines 2-3.

Claim 22 is rejected based on lack of positive antecedent basis of "said completion packet" on line 3, "the request packet of said first transaction" on lines 3-4.

Claims 23 and 24 are rejected because they depend on claim 22.

In claim 23, line 2, "includes further includes" should be corrected.

Claim 25 is rejected based on lack of positive antecedent basis of "said transaction descriptors" on lines 1-2.

Claim 26 is rejected based on lack of positive antecedent basis of "the respective request packet" on lines 2-3.

Claim 27 is rejected because it depends on claim 26.

In claim 28, line 2, "a means for is allotting ownership..." is unclear.

Claim 30 is rejected because it is not clear what is meant by "via s single interface..." on lines 10-11.

Claims 32-35 and 37-49 are rejected because they depend on claim 30.

Claim 32 is rejected based on lack of positive antecedent basis of "said first and second hubs" on lines 1-2.

Claim 35 is rejected based on lack of positive antecedent basis of "said first transaction" on lines 2-3.

Claim 37 is rejected based on lack of positive antecedent basis of "said completion packet" on line 3, "the request packet of said first transaction" on lines 3-4.

Claim 42 is rejected based on lack of positive antecedent basis of "said transaction descriptors" on lines 1-2.

Claim 43 is rejected based on lack of positive antecedent basis of "said request packet" on line 1 and "the respective request packet" on lines 2-3.

Claim 62 is rejected based on lack of positive antecedent basis of "the respective request packet" on line 3.

Claims 63-64 are rejected because they depend on claim 62.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 4-14, 16, 18-27, 29, 50, and 52-63 are rejected under 35 U.S.C. 102(e) as being anticipated by Bell, U.S. Pat. No. 6,088,370.

a. As to claims 1, 16, and 50, Bell discloses a single exclusive interface to transfer data directly between a memory control hub (MCH) (note Figure 1, controller 115 and column 2, lines 15-26) and a input/output control hub (ICH) (note Figure 1, bus expander bridge 120 and column 2, lines 26-32) within a computer system, comprising: a data signal path (note Figure 2A, data lines of point-to-point bus 200) to transmit data in packets via split transactions (note column 2, lines 55-59); and a set of command signals (note column 2, lines 46-48), wherein said interface provides a point-to-point connection between said MCH and said ICH (note Figure 1, bus 100 between controller 115 and bus expander bridge 120 and Figure 2A, point-to-point bus between controller 215 and bus expander bridge 220), exclusive of an external bus connected directly to the interface, and peripheral components only connected to MCH via a single

interface between the MCH and ICH (note Figure 1, wherein there is no external bus connected directly to the interface). Bell shows all of the elements recited in claims 1,16, and 50.

b. As to claims 4-9, 18-20, 21-24, 52-58, {18, 52}: Bell discloses that a first transaction is initiated on said interface with a request packet, subsequent to arbitration for ownership of said interface (note column 5, lines 8-30), {4, 19, 53}: wherein said request packet includes a transaction descriptor (note column 2, line 55 – column 3, line 10 and Figure 10A), {5, 20, 54}: wherein a completion packet is transmitted on said interface in response to said request packet of said first transaction (note column 2, line 55 – column 3, line 10 and Figure 10B), {6, 55}: wherein said request packet includes transaction descriptor and said completion packet includes a corresponding transaction descriptor (note column 14, line 51 – column 15, line 2), {7, 22, 56}: wherein a request packet for a second transaction can be transmitted across said interface prior to transmitting said completion packet in response to the request packet of said first transaction (i.e., inherent to the operation of a split transaction interfacing), {8, 23, 57}: wherein said data signal path is scalable (note column 11, line 58 – column 12, line 6 and column 13, line 12 – column 14, line 47), {9, 24, 58}: wherein packets are transmitted across said data signal path via a source synchronous clock mode (note column 3, lines 19-56).

c. As to claims 10, 11, 59, and 60, {10, 59}: Bell discloses that said interface includes a set of bi-directional data signals (note Figure 2A, XD), a first and second source synchronous strobe signal (note Figure 2A, two strobe signals, STB in both directions), a unidirectional arbitration signal (note Figure 2A, HRTS and XRTS), {11, 60}: wherein said interface further includes a system reset signal (note Figure 2A, RST signals), a common clock signal (note Figure 2A, CLK signals), and a voltage reference signal (i.e., inherent), but fails to explicitly disclose a bi-directional stop signal.

Olarig is being provided as evidence that a stop signal is inherent to the system of Bell, since Bell issues a retry in accordance with the PCI specification if a transaction cannot be carried out, and since Olarig teaches at column 10, lines 34-46 that in accordance with the PCI specification, a retry is indicated by the assertion of a STOP signal. Therefore, it is inherent to Bell that a STOP signal is present in order for a retry to be indicated.

d. As to claims 12, 25, and 61, Bell discloses that said transaction descriptors identify separate hubs within a hierarchy of multiple interfaces between at least three hubs (note Figure 1 and column 2, line 46 – column 3, line 10 and column 14, line 51 – column 15, line 2, wherein TIDs are necessary for all transactions and therefore would identify the hubs involved in the transactions).

e. As to claims 13, 26, and 62, Bell discloses that said request packet includes a field

indicating if a completion packet is required in response to the respective request packet (note Figure 10A, field RCOM).

f. As to claims 14, 27, and 63, Bell discloses that arbitration between said hubs is symmetric and distributed and that the interface includes a means for arbitrating between the hubs for ownership of the interface (note column 5, lines 8-30).

g. As to claim 29, the claim limitations have already been discussed with respect to claims 1, 2, 10, and 11 above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness

rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 2, 17, 30-35, 37-44,46,47 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell, 6,088,370 in view of Ram et al., 6,195,722 (hereinafter Ram).

a. As to claims 2, 17, and 51, Bell fails to disclose that said MCH and said ICH within said computer system are components within a chipset.

Ram discloses that the MCH and ICH are components within a chipset.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the MCH and ICH be components within a chipset, as Ram teaches, in the system of Bell so as to take advantage of the many well known benefits of chip integration, including low cost, less board space occupation and ease of manufacture and so as to allow for communication with peripherals attached to the chipset, as Ram teaches in column 1, lines 21-34.

b. As to claim 30, the claim limitations have already been discussed with respect to claim 1 above, with the exception of the computer system comprising a processor and a memory control hub coupled to the processor and at least one peripheral component coupled to the ICH.

Bell discloses that the computer system comprises at least one peripheral component coupled to the ICH (note column 2, lines 26-31), but fails to disclose a processor coupled to the memory control hub.

Ram discloses a processor coupled to the memory control hub (note Figure 1, elements 110).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have a processor coupled to the memory control hub, as Ram teaches, in the system of Bell so as to allow the processor to communicate with the memory control hub and the peripherals coupled to it, as Ram teaches in column 1, lines 12-16.

c. As to claim 31, Bell discloses that said peripheral component is a Peripheral Component Interconnect (PCI) agent (note column 2, lines 26-31).

d. As to claims 32-35 and 37-44, the claim limitations have already been discussed with respect to claims 2-5 and 7-14.

e. As to claim 46. Ram discloses that the computer system includes multiple processors.

f. As to claim 47, Bell discloses that the computer system further includes a third hub (note Figure 1, element 117) coupled to said ICH via an interface comprising: a bi-directional data signal path and a pair of source synchronous strobe signals, said data signal path transmits data in packets via split transactions, said packets including a request packet and completion packet, said request packet including a transaction descriptor; and a set of

command signals including unidirectional arbitration signal, a bi-directional **stop** signal, a system reset signal, a common clock signal, and a voltage reference signal (note Figure 2A and column 2, line 55 – column 3, line 10).

8. Claims 15, 28, and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell, 6,088,370 in view of Lambrecht et al., 5,951,664 (hereinafter Lambrecht).

As to claims 15, 28, and 64, Bell fails to disclose that a hub is allotted ownership of said interface up to a predetermined amount of time.

Lambrecht discloses that devices are allotted ownership of said interface up to a predetermined amount of time (note column 18, line 1 – column 19, line 11).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the hub allotted ownership of the interface up to a predetermined amount of time, as Lambrecht teaches, in the system of Bell so as to insure that the hub has access to the interface in accordance with its required bandwidth, as Lambrecht teaches in column 18, lines 2-5.

9. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bell, 6,088,370 in view Ram et al., 6,195,722 (hereinafter Ram), as applied to claims 2, 17, 30-35, 37-44, and 51 above, and further in view of Lambrecht et al., 5,951,664 (hereinafter Lambrecht).

As to claim 45, the claim limitations have already been discussed with respect to claims 15, 28, and 64 above.

10. Claims 48 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell, 6,088,370 in view of Ram et al., 6,195,722 (hereinafter Ram), as applied to claims 2, 17, 30-35, 37-44, and 51 above, and further in view of Gulick et al., 6,148,357 (hereinafter Gulick).

As to claims 48 and 49, Bell fails to disclose that the processor and the MCH of said computer system, are integrated on a single semiconductor unit or that the MCH and a graphics unit of said computer system, are integrated on a single semiconductor unit.

Gulick discloses that the processor (i.e., CPU) and the MCH (i.e., memory controller 1505) of said computer system are integrated on a single semiconductor unit (i.e., 1701) and that the MCH and a graphics unit (i.e., 1401) of said computer system are integrated on a single semiconductor unit (note Figure 17).

It would have been obvious to one of ordinary skill in the art at the time of the invention to integrate the CPU and MCH and the MCH and graphics units of Bell onto a single semiconductor circuit, as Gulick teaches, so as to provide the advantage of greater system integration resulting in the elimination of a separate graphics controller circuit, as Gulick teaches at column 17, lines 1-4, and also the elimination of a separate memory controller circuit.

11. Claims 65 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell, 6,088,370 in view of Gulick et al., 6,148,357 (hereinafter Gulick).

As to claims 66, the claimed elements have already been discussed with respect to claims 48 and 49 above.

Response to Arguments

12. Applicant's arguments with respect to claims 1,2,4-20,22-30,32-35 and 37-66 have been considered but are moot in view of the new ground(s) of rejection.

Applicant notes that claims 4 and 32 were rejected under 35 USC §112, 2nd paragraph, however no amendments were made to these claims and no argument was made regarding the

rejection. On closer inspection of the claims there are numerous other instances of antecedent basis problems and other issues as outlined above in the rejection.

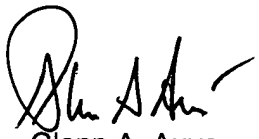
With respect to the rejections under 35 USC §103(a) applicant argues that the addition of the term "a single exclusive interface" to the claims renders them patentable over the prior art. Applicant argues that Bell does not show a single exclusive interface but rather shows a controller coupled to multiple bus expanders to provide multiple interfaces. However, between one bus expander, for example bridge 120, and the controller 115 there is but a single, exclusive interface shown by lines 100. This portion of the embodiment shown by Bell appears to clearly meet the claimed limitation of a single exclusive interface, and therefore applicant's arguments in this regard are not persuasive. It is also noted that the rejection of some of the claims has been shifted to one under 35 USC § 102(e) since the limitation noted by the examiner as not being present in Bell in the previous rejection is not contained in the claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (571) 272-3623. The examiner can normally be reached on M-F 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
28 February 2005